Impact of Random Telegraph Noise Profiles on Drain-Current Fluctuation During Dynamic Gate Bias

doi: 10.1109/LED.2013.2288981

Impact of Random Telegraph Noise Profiles on Drain-Current Fluctuation during Dynamic Gate Bias

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***Abstract*—The influence of random telegraph noise (RTN) in MOSFETs on drain current (I_d) during the rise/fall edges of the pulsed gate voltage (V_g) cycle was investigated. We have revealed for the first time that the existence of RTN increases I_d fluctuations under dynamic V_g by making a comparison between FETs with and without RTN. The initial trap occupation states before varying V_g, which are governed by the RTN profiles, significantly affect the I_d values during the rise/fall edges of V_g. The revealed effects of RTN with different profiles on I_d under dynamic V_g will be useful for designing ultra-high speed circuits.**

***Index Terms*— MOSFETs, Random Telegraph Noise, Dynamic Gate Bias**

I. Introduction

As metal-oxide-semiconductor (MOS) field-effect transistors (FETs) are scaled down for further integration, the relative impact of randomly placed discrete charges (oxide traps, interface states, and fixed charges) on device characteristics increases significantly, leading to circuit failure. One of the principal issues that has been studied is that of random telegraph noise (RTN) because of its increasing influence with shrinkage of the device area.[1-4] Recently, RTN has attracted much attention in digital circuits, since it causes threshold voltage (V_{th}) variation and directly degrades circuit reliability.[4] For example, the operation of SRAM devices depends on the current balance between FETs, and thus is very sensitive to V_{th} shifts.[5] The RTN-induced failure of SRAMs during accelerated testing was observed.[6] The influence of RTN during continuous ac cycles and the relationship to hysteresis behavior are also reported.[7]

In the operation of ultrahigh-speed circuits, the rectangular shape of the ideal large-signal is rounded as the clock frequency increases to several GHz, so that the relative proportion of the rise and fall edges to the 'on' state becomes significant. However, the effect of RTN during the rise and fall edges is not fully understood yet. Therefore, it is important to investigate the impact of RTN on dynamic drain current (I_d) fluctuations during the rise/fall edges of the pulsed gate voltage (V_g).

In this work, the impact of RTN on I_d fluctuations under dynamic gate bias is presented by making comparisons between FETs w/o and with RTN of different profiles. We have revealed that the profiles of RTN determine the I_d fluctuation during the rise and fall edges of pulsed V_g.

II. Experimental Procedure

We used planar-type n-FETs with a poly-Si/high-k gate stack structure for the characterization of the impact of RTN on I_d fluctuations. An HfO_2 gate dielectric film with a 0.8-nm-thick SiO_2 interfacial layer was adopted for the gate-stack structure. The equivalent oxide thickness of the samples was 1.2 nm. The gate length and width are 140 and 200 nm, respectively. Fast IV units (Agilent B1530A) were employed for monitoring the I_d fluctuations. Either constant dc biases or dynamic V_g pulsed inputs were applied on the FETs, while the drain voltage was maintained at 1 V. In order to obtain fast, accurate I_d responses to the fast dynamic V_g, a common ground was taken at the measuring probe tips for the source, the drain, the gate and the substrate of the FET. We have characterized the noise properties of 16 FETs, from which three representative FETs are shown, namely w/o RTN, with symmetric RTN, and with asymmetric RTN.

III. Dynamic fluctuation

For FETs with RTN, I_d exhibits high and low levels due to the emission and capture states of the traps, respectively. The time constants of RTN (τ_c and τ_e) are defined as the average duration times of the high and low I_d states, respectively. The values of τ_c and τ_e are generally used to understand the characteristics of the traps, such as trap energy and trap depth.[4] We focus on the symmetry of the RTN profiles, which is reflected in the ratio of capture-to-emission times (τ_c/τ_e). The τ_c/τ_e ratio is governed by the difference between the trap energy E_T and the Fermi level E_F, as shown in the following equation[8]

$$\frac{\tau_c}{\tau_e} = \exp\left(\frac{E_T - E_F}{k_B T}\right) \quad (1)$$

where k_B is the Boltzmann constant and T is temperature. A trap with different E_T - E_F exhibits varied symmetry.

We investigated I_d fluctuations for FETs with RTN of

Manuscript received October 31, 2013. This work was supported by JST-CREST. W. Feng, M. Niwa, K. Yamada, and K. Ohmori are with the Graduate School of Pure and Applied Sciences, University of Tsukuba, 1-1-1 Tennnodai, Tsukuba, Ibaraki 305-8573, Japan and Core Research for Evolutional Science and Technology, Japan Science and Technology Agency (JST-CREST), Chiyoda, Tokyo 102-0075, Japan (e-mail: wei.feng@aist.go.jp).

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different profiles. In these experiments, RTN is observed in the V_g ranges from V_{th} + 0.1 V to V_{th} + 0.4 V for two devices, i.e., FET-A and FET-B. The V_{th} values for FET-A and -B are 0.77 V and 0.76 V, respectively. For the same condition of $V_g = V_{th}$ + 0.25 V, the FET-A exhibits symmetric RTN (Fig. 1 (a)), while FET-B shows asymmetric RTN (Fig. 1 (b)). These symmetric and asymmetric characteristics of RTN are more clearly demonstrated in the I_d histograms Fig. 1 (c) and (d), respectively. Two primary I_d peaks are observed in both cases, corresponding to the capture and emission conditions of RTN. Figure 1 (c) shows two peaks with similar I_d counts for FET-A, reflecting a τ_c/τ_e ratio of 0.84. For FET-B, the τ_c/τ_e ratio is evaluated to be 4.2.

The symmetry of RTN, which is reflected in the τ_c/τ_e ratio, depends on V_g and plays a crucial role in determining I_d fluctuations under dc bias. Taking FET-B as an example, the changes in the time constants (τ_c and τ_e) of RTN and the corresponding standard deviation of the I_d (σ_{Id}) values as functions of I_d and V_g are shown in Fig. 2. The σ_{Id} value is strongly affected by the symmetry of RTN, showing a maximum at $\tau_c/\tau_e = 1$.[9] The σ_{Id} exhibits a maximum at $V_g - V_{th} = 0.3$ V, where τ_e is almost at the same level as τ_c.

I_d fluctuations were investigated under dynamic V_g. The waveforms of V_g and the corresponding I_d for 400 cycles are shown in Fig. 3 (a). V_g is programmed to rise from the lower gate voltage (V_{gL}) to the higher gate voltage (V_{gH}) with the transition time (t_{TR}) ranging from 10 μs to 10 ms. V_g remains at V_{gH} for 10 μs, and then decreases back to V_{gL} with the same t_{TR}. According to the condition for the appearance of RTN in FETs under constant dc bias, the values of V_{gL} and V_{gH} are set to be V_{th} + 0.1 V and V_{th} + 0.4 V, respectively. In order to make a fair comparison between the dynamic I_d fluctuations during the rise and fall edges, the I_d fluctuation was extracted at the middle points V_{gM} (= V_{th} + 0.25 V) between V_{gL} and V_{gH} to ensure the same transition time from V_{gL} and V_{gH} to the evaluating points, as shown in the magnified figure (Fig. 3 (b)). Figure 3 (c) shows the extracted I_d values for 400 cycles. The cycle is repeated 200-4400 times to enable sufficient sampling of I_d for fluctuation analysis.

The influence of RTN on I_d during the gate voltage ramping (rise/fall) was examined by comparing the I_d fluctuations among the FETs w/o, with symmetric, and with asymmetric RTN. Figure 4 (a) shows the σ_{Id} of the FETs as a function of t_{TR}. The σ_{Id} levels under dc bias for the FETs with and w/o RTN are added as references. Note that the magnitude of the asymmetric RTN (FET-B) is larger than that of the symmetric RTN (FET-A) as shown in Fig. 1. Therefore, the σ_{Id} level under dc bias of the FET with asymmetric RTN is higher than that of the FET with symmetric RTN in Fig. 4 (a). As expected from the previous discussion in Fig. 2 (b), the appearance of RTN increases σ_{Id}. The possibility of two trap states for the FETs with RTN results in larger values of dynamic fluctuation σ_{Id} than that without RTN, reflecting the magnitudes of deviation under dc bias.

The increases in σ_{Id} values with t_{TR} for FET-A and -B were investigated in detail. The I_d values of the FETs with RTN depend on the trap occupation states. Under dynamic V_g, there are two predominant factors for determining I_d fluctuations: the initial trap occupation states and the trap occupation states change probabilities from initial V_g to V_{gM}. The trap occupation

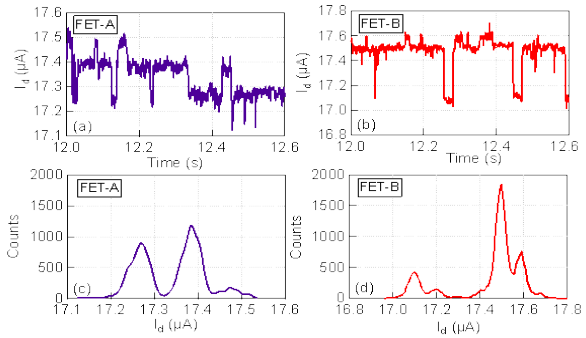

Fig. 1. (Color online) The I_d fluctuation of (a) FET-A with symmetric RTN and (b) FET-B with asymmetric RTN measured under constant dc bias. I_d distribution of (c) FET-A and (d) FET-B.

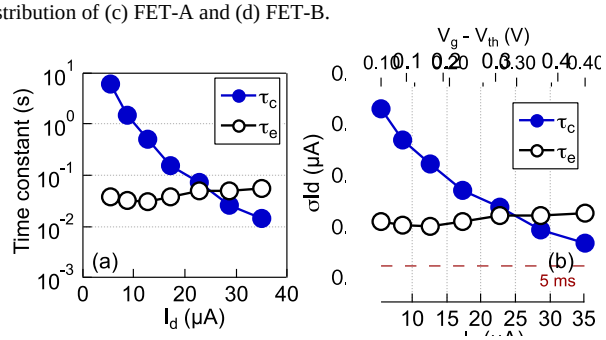

Fig. 2. (Color online) (a) Time constant of RTN and (b) σ_{Id} of FET-B under dc bias as a function of I_d and gate overdrive V_g - V_{th}. Note that the upper scales in (a) and (b) are not linear.

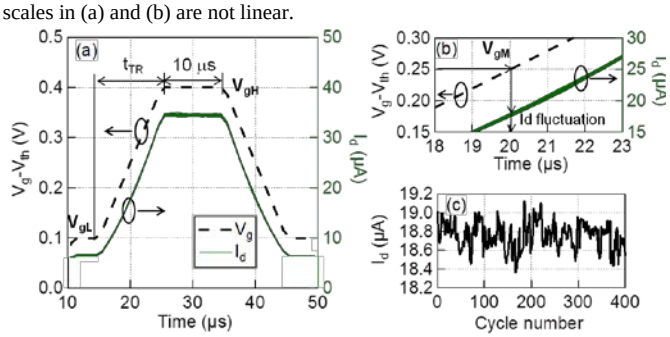

Fig. 3. (Color online) (a) V_g pulse sequence and experimental data of I_d as a function of time with t_{TR} = 10 μs. (b) Magnified figure demonstrates the evaluation of the I_d fluctuation of repeated V_g pulses at V_{gM}. (c) Dynamic I_d fluctuation values at V_{gM} as a function of cycle number.

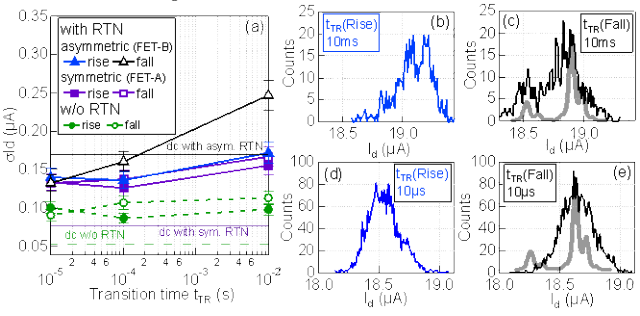

Fig. 4. (Color online) (a) Comparison of σ_{Id} of the FET w/o RTN and with RTN of different profiles. Distribution of dynamic I_d of the FET with asymmetric RTN in FET-B is shown for (b) rise and (c) fall edges with t_{TR} = 10 ms and (d) rise and (e) fall edges of t_{TR} = 10 μs.

states change due to the capture/emission of electrons, and the capture/emission probability depends on the ratio of the duration time ($t_{TR}/2$) to the time constants of RTN.

For FET-A, the values of τ_c/τ_e under constant dc bias are 1.5, 0.84, and 0.4 for V_{gL}, V_{gM}, and V_{gH}, respectively. As τ_c/τ_e is closer to 1 at V_{gM} than that at V_{gL}, according to previous discussion in Fig. 2, σ_{Id} under constant dc bias of V_{gM} is larger than that of V_{gL}. When V_g rises from V_{gL} to V_{gM}, σ_{Id} changes towards to a larger value with the capture/emission of electrons. The capture/emission probability increases with t_{TR}. Therefore, σ_{Id} at V_{gM} on the rise edges increases with t_{TR}. For the same reason, σ_{Id} at V_{gM} of the fall edges also increases with t_{TR}.

For the FET-B, since τ_c/τ_e is closer to 1 at V_{gM} than that at V_{gL} or V_{gH} (Fig. 2(a)), a similar feature to that of FET-A is observed. However, as t_{TR} becomes longer, the σ_{Id} value for the fall edges increases dramatically. To reveal the origin of the σ_{Id} values, a histogram of dynamic I_d for FET-B was evaluated for the rise and fall edges at t_{TR} = 10 ms and 10 μs (Fig. 4 (b)-(e)). For the case of t_{TR} = 10 ms, the I_d distribution at the rise edges mainly shows one peak, while that for the fall edges is composed of two peaks. Therefore, σ_{Id} of the fall edges shows larger values. The I_d distribution under constant dc bias is superimposed to the I_d histogram of the fall edges, as shown by the grey line with its horizontal scale shifted. We emphasize that the difference in peak positions of I_d distribution under dynamic V_g is similar to that of constant dc bias, indicating the appearance of RTN during the fall edge. Note that the I_d distribution of dynamic V_g is broader than that under dc bias, resulting from additional I_d fluctuations due to the dynamic transition of V_g. With a shorter t_{TR} of 10 μs, the I_d distribution width becomes narrower than that of the 10 ms case. The I_d distribution of the rise edges remains a single peak-shaped structure (Fig. 4 (d)). However, the two peak-shaped structure of the I_d distribution when t_{TR} = 10 ms on the fall edges becomes one peak-shaped at 10 μs, as shown in Fig. 4 (e).

Here we consider the origins of the one or two peaks in the I_d distribution. As τ_c is the time for the empty states, the value of τ_c/τ_e indicates the possibility of empty traps. With a τ_c/τ_e value of 170 at V_{gL}, the possibility of empty traps is 99.4%. For t_{TR} = 10 ms, the time for capturing electrons during the rise edges ($t_{TR}/2$) is less one order smaller than the τ_c values as shown in Fig. 2 (a). Therefore, the trap occupation state at V_{gM} on the rise edges is mostly empty, resulting in a single peak-shaped structure for the I_d distribution in Fig. 4 (b). The trapping of electrons changes the trap occupation states from empty to filled, which increases σ_{Id}. The electron capture probability is larger for longer t_{TR}, resulting in an increase in σ_{Id}.

In the case of the fall edges, the value of τ_c/τ_e at V_{gH} decreases to 0.26, indicating the possible existence of both empty and filled states. Thus, there are two kinds of initial trap occupation states for the fall edges, which result in a histogram with two peaks (Fig. 4 (c)). For a shorter rising time t_{TR} of 10 μs, which is three orders smaller than the τ_c value in Fig. 2 (a), the capture probability decreases to the order of 1/1000. Therefore, the trap occupation states remain the same as that at V_{gL} (empty) with a high probability for V_{gH}. Hence, one initial trap occupation state at V_{gH} results in a single peak-shaped structure for the I_d distribution at the fall edges (Fig. 4 (e)).

Two kinds of initial trap occupancy states for the repeated V_g pulses lead to a two peak-shaped structure for the dynamic I_d distribution, resulting in a larger σ_{Id} than the case of the single initial trap state. Therefore, the variation of the initial occupancy trap states is essential for the I_d fluctuation during the rise and fall edges of dynamic V_g.

IV. Conclusion

We have investigated the influence of RTN during dynamic pulses upon I_d fluctuation, focusing on the rise and fall edges. We have found for the first time that RTN increases dynamic I_d fluctuations, even when the transition time is significantly shorter than the time constants (τ_c and τ_e) of RTN. The initial trap occupation states prior to the rise/fall edges of V_g are reflected in the I_d distribution during rise/fall ramping. The initial trap occupation states are governed by the symmetry of the RTN profiles (τ_c/τ_e) in addition to the magnitudes of τ_c and τ_e. Therefore, the profiles of RTN are essential for determining the I_d fluctuation during the dynamic V_g.

These results imply an additional factor in the I_d noise modeling of FETs for designing an ultra-high speed circuits, where the proportion of the rise/fall time to a single large-signal clock is not negligible.

Acknowledgment

The authors would like to thank Innovative Center Advanced Nanodevices (ICAN) of Advanced Industrial Science and Technology (AIST) for the continuous support.

References

[1] R. E. Howard, L. D. Jackel, P. M. Mankiewich, and W. J. Skocpol, “Electrons in silicon microstructures,” Science, vol. 231, no. 4736, pp. 346-349, Jan. 1986.

[2] K. Ohmori, W. Feng, S. Sato, R. Hettiarachchi, M. Sato, T. Matsuki, K. Kakushima, H. Iwai, and K. Yamada, “Direct real-time observation of channel potential fluctuation correlated to random telegraph noise of drain current using nanowire MOSFETs with four-probe terminals,” in *Proc. 2011 Symp. VLSI Technology*, 2011, pp.202-203.

[3] K. Takeuchi, “Impact of discrete-charge-induced variability on scaled MOS devices,” IEICE Trans. Electron., vol. E95-C, no. 4, pp. 414–420, Apr. 2012.

[4] S. T. Martin, G. P. Li, E. Worley, and J. White, “The gate bias and geometry dependence of random telegraph signal amplitudes,” Electron Device Letters, vol. 18, no. 9, pp.444-446, Sep. 1997.

[5] S. O. Toh, T.-J. King Liu, and B. Nikolić, “Impact of random telegraph signaling noise on SRAM stability,” in *Proc. Symp. VLSI Technology*, 2011, pp. 204-205.

[6] K. Takeuchi, T. Nagumo, K. Takeda, S. Asayama, S. Yokogawa, K. Imai, and Y. Hayashi, “Direct observation of RTN-induced SRAM failure by accelerated testing and its application to product reliability assessment,” in *Proc. Symp. VLSI Technology*, 2010, pp. 189-190.

[7] H. Miki, N. Tega, Z. Ren, C. P. D’Emic, Y. Zhu, D. J. Frank, M. A. Guillorn, D. Park, W. Haensch, and K. Torii, “Hysteretic drain-current behavior due to random telegraph noise in scaled-down FETs with high-k/metal-gate stacks,” in *Proc. IEDM*, 2010, pp. 620-623.

[8] M. J. Kirton, and M. J. Uren, “Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/*f*) noise,” Advances in Physics, vol. 38, no.4, pp. 367-468, May. 1989.

[9] N. Zanolla, D. Šiprak, M. Tiebout, P. Baumgartner, E. Sangiorgi, and C. Fiegna, “Reduction of RTS noise in small-Area MOSFETs under switched bias conditions and forward substrate bias,” Trans. on Electron Devices, vol. 57, no. 5, pp. 1119–1128, May 2010.